Sub B1 Concl'd

an upper surface having only first and second rows of conductive pads disposed thereon and extending along respective ones of the opposite sides of the packaged chips; and

a lower surface having only third and fourth rows of conductive pads disposed thereon and extending along respective ones of the opposite sides of the packaged chips;

the leads of one of the packaged chips being electrically connected to respective ones of the conductive pads of the first and second rows disposed on the upper surface of the frame, with the leads of one of the packaged chips being electrically connected to respective ones of the conductive pads of the third and fourth rows disposed on the lower surface of the frame.

8. (New) The chip stack of Claim 7 wherein the packaged chips each comprise a TSOP packaged chip.

Sub B2

9. (New) The chip stack of Claim 7 wherein the conductive pads of the first and second rows disposed on the upper surface of the frame are electrically connected to respective ones of the conductive pads of the third and fourth rows disposed on the lower surface of the frame.

REMARKS

By this Preliminary Amendment, Applicant has added new Claims 7-9 into prosecution. Claims 1-6 as currently included in Applicant's U.S. Patent No. 5,869,353 (the "'353 Patent") are all method claims. New Claims 7-10 added into prosecution via this Preliminary Amendment are all apparatus claims. Since no apparatus claims were prosecuted in U.S. Application Serial No.